IN THE SPECIFICATION

Please replace the paragraph beginning at line 15 on page 2 with the following paragraph.

As computer systems started to utilize more graphic images and video conferencing became more desirable, the communication of video data has become important over both LANs and WANs. While separate means for communication of video between end users could have been developed, it is desirable to simultaneously ~~communication~~ **communicate** video data, audio data, and digital data across a LAN and a WAN.

Please replace the paragraph beginning at line 15 on page 5 with the following paragraph.

ATM networks communicate using cell switching which is a form of ~~Asynchronous~~ **asynchronous** time division multiplexing. ~~The cell~~ **Cells** used in ATM are of a fixed length as opposed to packet switching which uses variable length data packets.

Please replace the paragraph beginning at line 6 on page 18 with the following paragraph.

A novel aspect of the ATM module 101, which utilizes an ATM processor 120 to fetch/forward ATM cells from/to ports (e.g. UTOPIA Level 2 port 108, Cell I/F port 106 etc.) and functions (e.g. AAL2 SAR 102, AAL5 SAR 105, Cell Buffer 104, etc.), allows for a function/feature rich ATM solution as well as enhanced system performance by reducing the overhead on the host. As previously mentioned, these functions can include ATM switching, Quality of Service (QoS), and ~~operation~~ **Operation** and Maintenance (OAM) processing.

Please replace the paragraph beginning at line 5 on page 29 with the following paragraph.

One disadvantage of this type of system is that data transmitted or received must be written on the system bus twice (once between the host processor and the DSP, and once between

the host processor and the ATM transport hardware), resulting in system performance degradation. Another disadvantage is that very software intensive functions must be performed for AAL2 transmit and receive, such as CRC and parity calculation. Hence, a relatively powerful, host processor must ~~he~~ be used compared to if the AAL2 transmit and receive function had been done in dedicated hardware. Because of at least the aforementioned disadvantages, this architecture also does not scale very well to dense voice solutions.

Please replace the paragraph beginning at line 14 on page 37 with the following paragraph.

More particularly, referring to Figure 5 there is illustrated a function block diagram of an ~~AAL~~ AAL2 receiver 950 in accordance with an exemplary embodiment of the present invention. The AAL2 receiver 950 can be implemented in hardware in the ATM module 102. The AAL2 receiver 950 has two sets of DMAs associated with the AAL2 RX DMA 515 which are directly interfacing with the DSP(s) ~~160~~ 412 & 413 and the host ~~190~~ 414 (i.e. processing element): DSP DMA(s) - writes AAL2 voice packets to the DSP(s) ~~160~~ 412 & 413 and HOST DMA - writes AAL2 signaling/management packets to the host ~~190~~ 414.

Please replace the paragraph beginning at line 9 on page 38 with the following paragraph.

The Reassembly Engine 520 checks the CPS packet header's HEC, and determines if the CPS-packet(s) should be forwarded to one of the DSPs (A or B) Rx FIFOs (540, 541) or the Rx Host FIFO 530 as follows. The AAL2 receive engine allows the host ~~190~~ 414 to configure CPS-packets to be filtered to the host ~~190~~ 414 on CID or UUI information. Hence, the host ~~190~~ 414 can receive CPS-signaling packets and peer-to-peer layer management packets. If a match was made in the CID Filter 550, then the packet will be forwarded to the host ~~190~~ 414 and the UUI Filter 560 is not interrogated. If no match was made in the CID Filter 550, the UUI Filter 560 is searched. If a match is made in the UUI Filter 560 the packet will either be forwarded to the Host DMA or discarded. (The UUI Filter has a feature that allows the host to discard packets based on the UUI.) Otherwise, if a CPS-packet's CID matches a CID in the AAL2 Rx LUT (LookUp

Table) 580, the packet is forwarded to one of the 9 channels (8 voice channels and one host channel) in the Rx DMA RAM 590 according to the logical channel number associated with that particular CID. The entries in the LUT 580 are updated when the host software adds an AAL2 channel via the AAL2 Channel Configuration Register.

Please replace the paragraph beginning at line 7 on page 39 with the following paragraph.

After the CPS-packet(s) have been encapsulated on an CPS-packet boundary, the AAL2 Rx DMA 515 will write the data into either Rx FIFO A 540, Rx FIFO B 541, or the Rx Host FIFO 530. By monitoring the FIFO's read and write pointers, the DSP(s) ~~160~~ 412 & 413 and host ~~190~~ 414 can determine when CPS packets are available to them.

Please replace the paragraph beginning at line 16 on page 39 with the following paragraph.

Further, communication between the functional blocks (i.e. DSP(s) ~~160~~ 412 & 413, Host ~~190~~ 414 and AAL2 950) are minimized due to the fact that the protocol between the functions is drastically simplified with the AAL2 Receiver 950 directly interfaced with the DSP(s) ~~160~~ 412 & 413. Latency is minimized because of the direct connection to the DSP FIFO. The data is only written once across the system bus. An end result is overall improved system performance.